SSB501A
Multiprotocol Bluetooth 5/ANT Module Datasheet

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Product name	Type number	Product status
Multiprotocol Bluetooth 5.0/ANT Low Energy Module	SSB501A-CSEI (09267)	Mass Production
	SSB501A-XXPI (0926701)	
	SSB501A-CSPI (0926702)	

Contents

1 General Description....4
2 Applications....4
3 Features....5
4 Application Block Diagram....6
5 Interfaces....6
5.1 Power Supply....6
5.2 System Function Interfaces....6
5.2.1 GPIOs....6
5.2.2 Two-wire Interface (I2C Compatible)....7
5.2.3 Flash Program I/Os....7
5.2.4 Serial Peripheral Interface....7
5.2.5 UARTs....8
5.2.6 Analog to Digital Converter (ADC)....8
5.2.7 Low Power Comparator (LPCOMP)....9
5.2.8 Reset....9
5.2.9 NFC....9
6 Module Specifications....10
7 Module Pinout and Pin Description....11
7.1 Module Pinout....11
7.2 Pin Description....12
8 PCB Design Guide....13
9 PCB Footprint and Dimensions....13
10 Electrical Characteristics....14
10.1 Absolute Maximum Ratings....14
10.2 Recommended Operation Ratings....14
10.3 Current....15
11 Manufacturing Process Recommendations....15
12 Packaging Specification....16
13 Ordering Information....16
14 Revision History....16

1 General Description

Ready for Bluetooth 5 and high grade IoT security

The SSB501A is an advanced, highly flexible single chip solution for today's increasingly demanding ULP wireless applications for connected devices on our person, connected living environments and the IoT at large. It is designed ready for the major feature advancements of Bluetooth® 5 and takes advantage of Bluetooth 5's increased performance capabilities which include long range and high throughput modes. Inherent industry-grade security is essential in today's applications.

Bluetooth 5 – Bluetooth low energy further and faster

The nRF52840 is ready to take advantage of the considerable performance improvements for Bluetooth low energy with the arrival of the Bluetooth 5 specification. Of greatest importance is the support for longer range (up to x4 compared to Bluetooth 4.x) and doubling of on-air data-rate, up to 2Mbs from 1Mbs in Bluetooth 4.x

Wide protocol support with addition of 802.15.4

The 802.15.4 PHY and MAC layers are supported natively on the nRF52840. This allows nRF52840 to be used in a wide range of home and industrial sensor network applications as it supports two of the most popular wireless sensor standards in use today, Bluetooth low energy and 802.15.4 derivatives. This adds to the already existing radio support for Bluetooth low energy, ANT/ANT+ and 2.4GHz for proprietary.

Figure 1: SSB501A Top View

2 Applications

- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Interactive entertainment devices
  - Remote control
  - 3D Glasses

Gaming controller

- Advanced wearables

  Connected watches

  Advanced personal fitness devices

  Wearables with wireless payment

  Connected Health

  Virtual/Augmented Reality applications

- IoT

  Smart Home sensors and controllers

  Industrial IoT sensors and controllers

3 Features

- Bluetooth 5 ready multi-protocol radio
- Bluetooth 5 datarate support: 2Mbs, 1Mbs, 500Kbs, 125Kbs
- Support ANT Protocol
- 32-bit ARM Cortex-M4F @ 64MHz
- Up to 111 dB link budget for Bluetooth long range mode
- NFC-A on-chip
- Programmable output power from +8dBm to -20dBm
- -96dBm Sensitivity for Bluetooth low energy
- RSSI
- Wide supply voltage range +5.5v to 1.7v
- Full selection of interfaces SPI/UART/PWM
- Programmable Peripheral Interface - PPI
- High speed SPI interface 32MHz
- EasyDMA for all digital interfaces
- 12bit/200K SPS ADC
- 128 bit AES/ECB/CCM/AAR co-processor
- 20 General Purpose I/O pins
- SPI Master/Slave
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- RoHS compliance (Lead-free)
- FCC,CE compliance

4 Application Block Diagram

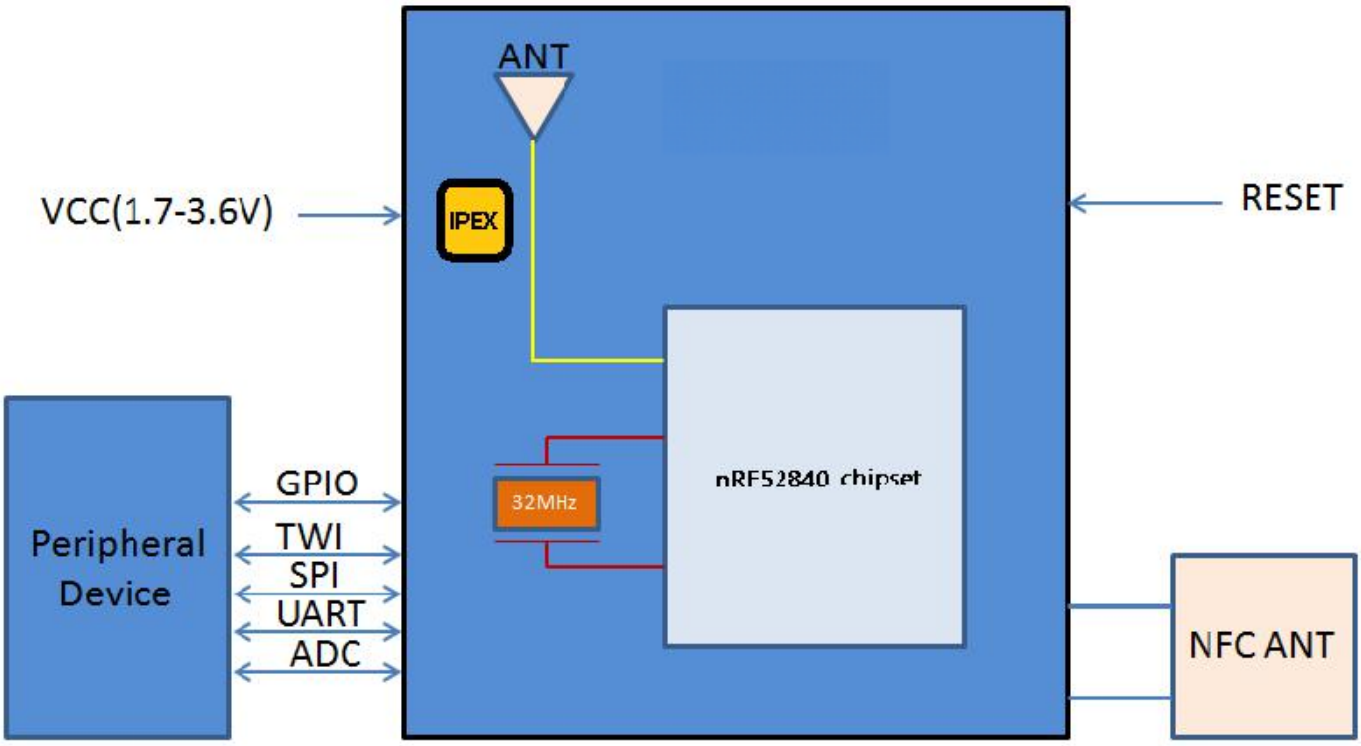

Figure 3: SSB501A Block Diagram

5 Interfaces

5.1 Power Supply

Regulated power for the SSB501A is required. The input voltage VCC range should be 1.7V to 3.6V.

Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF).

It can reduce the noise from power supply and increase power stability.

5.2 System Function Interfaces

5.2.1 GPIOs

The general purpose I/O is organized as one port with up to 20 I/Os enabling access and control of up to 19 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

1、Input/output direction

2、Output drive strength

3、Internal pull-up and pull-down resistors

4、Wake-up from high or low level triggers on all pins

5、Trigger interrupt on all pins

6、All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

7、All pins can be individually configured to carry serial interface or quadrature demodulator signals

8、All pins can be configured as PWM signal.

9、There are 6 ADC/LPCOMP input in the 20 I/Os.

5.2.2 Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps ,250kbps and 400 kbps. The module has 2 TWI ports and they properties like following table.

Instance	Master/Slave
TWI0	Master
TWI1	Master

Table5-1: TWI Pin Share Scheme

Note： I2C:Inter－Integrated Circuit

5.2.3 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI

Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line can be chosen from any GPIOs on the device and configed independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral support SPI mode 0,1,2,and 3.The module have 3 SPI ports and theirs they properties are as below:

Instance	Master/Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

Table5-2: SPI Properties

5.2.5 UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. Support the following baudrate in bps unit:

1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200/230400/250000/460800/ 921600/1000000.

Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configured independently.

5.2.6 Analog to Digital Converter (ADC)

The 12 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

SKB501 Pin Number	Pin Number	Description
6	P0.28	Digital I/O; Analog input 4
7	P0.29	Digital I/O; Analog input 5

8	P0.30	Digital I/O; Analog input 6
9	P0.31	Digital I/O; Analog input 7
11	P0.02	Digital I/O; Analog input 2
12	P0.03	Digital I/O; Analog input 3

Table5-3: ADC Pins

5.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8 Reset

The reset pin of the SSB501A module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the parameters of the current setting will not be ANT .

5.2.9 NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

• NFC-A listen mode operation

• 13.56 MHz input frequency

• Bit rate 106 kbps

• Wake-on-field low power field detection (SENSE) mode

• Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum

• Programmable frame timing controller

• Integrated automatic collision resolution, CRC and parity functions

SKB501 Pin Number	Pin Number	Description
16	P0.10	Digital I/O; NFC2
17	P0.09	Digital I/O; NFC1

Table5-4: ADC Pins

6 Module Specifications

Hardware Features	
Model	SSB501A
Antenna Type	PCB Antenna or IPEX connector
Chipset Solution	nRF52840
Voltage	1.7V~3.6V
Dimension(L×W×H)	17.4×13.7×1.9 mm
Wireless Features	
Wireless Standards	Bluetooth ® 5.0,ANT
Frequency Range	2400MHz---2483.5MHz
Data Rates	Uncoded:1Mbps/2Mbps,Coded:125kbps(S=8)/500kbps(S=2)
Modulation Technique	GFSK Modulation
Wireless Security	AES HW Encryption
Transmit Power	Tx Power -20 to +8 dBm in 4 dB Steps
Work Mode	Central/Peripheral
Others	
Certification	RoHS
Environment	Operating Temperature: -40℃~85℃
	Storage Temperature: -40℃~125℃
	Operating Humidity: 10%~90% Non-condensing
	Storage Humidity: 5%~90% Non-condensing

7 Module Pinout and Pin Description

7.1 Module Pinout

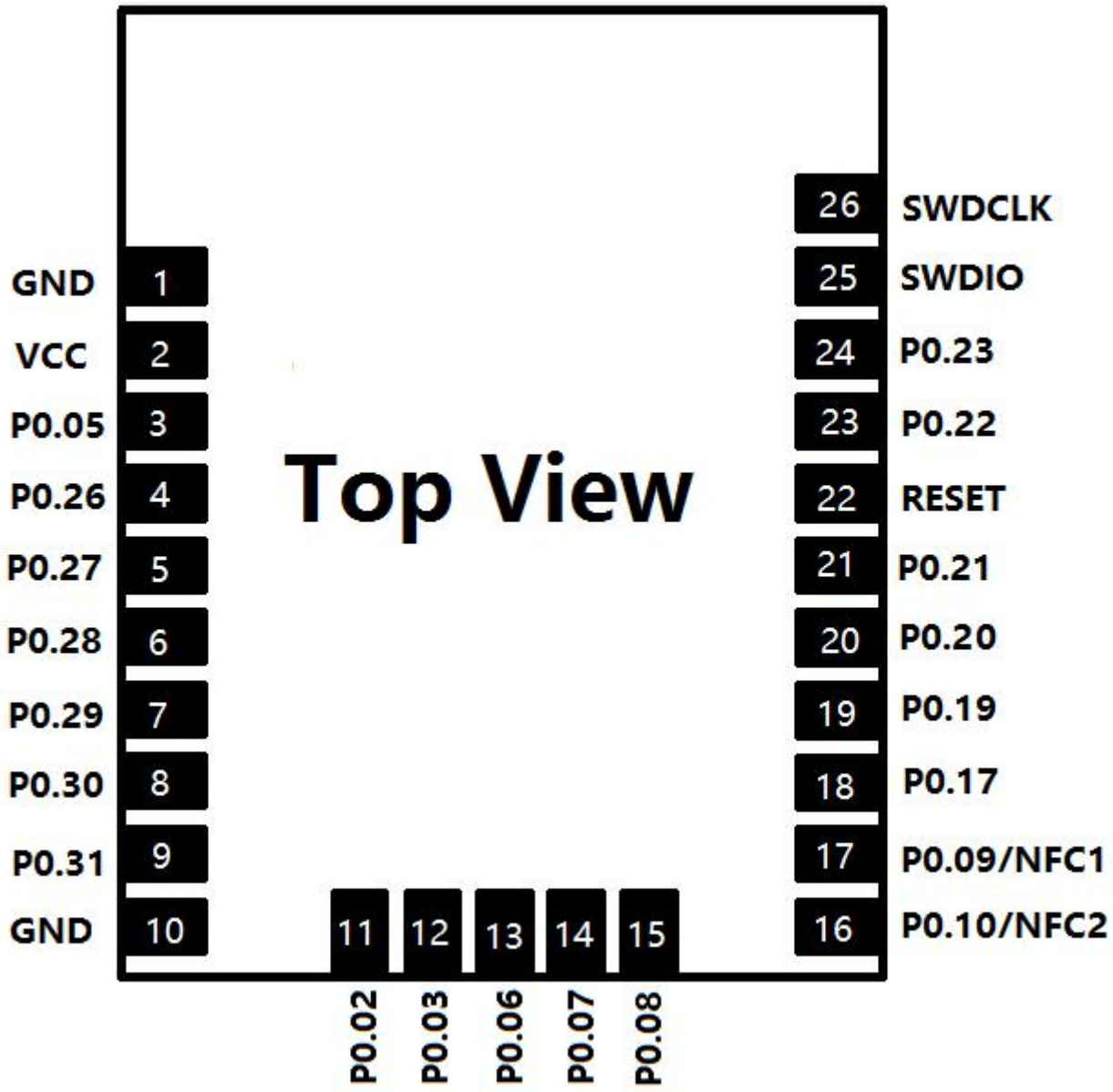

Figure 4: SSB501A Module Pinout

7.2 Pin Description

Pin No.	Pin Name	Description	Remark
1	GND	Ground	
2	VCC	Main Power Supply	1.7V to 3.6V
3	P0.05	Digital I/O; UART RTS	Digital I/O
4	P0.26	Digital I/O; I2C_SDA	Digital I/O
5	P0.27	Digital I/O; I2C_SCL	Digital I/O
6	P0.28	Digital I/O; Analog input	ADC/LPCOMP input 4
7	P0.29	Digital I/O; Analog input	ADC/LPCOMP input 5
8	P0.30	Digital I/O; Analog input	ADC/LPCOMP input 6
9	P0.31	Digital I/O; Analog input	ADC/LPCOMP input 7
10	GND	Ground	
11	P0.02	Digital I/O; Analog input	ADC/LPCOMP input 0
12	P0.03	Digital I/O; UART TXD	Digital I/O
13	P0.06	Digital I/O; UART RXD	Digital I/O(/ADC/LPCOMP input1）
14	P0.07	Digital I/O; UART CTS	Digital I/O
15	P0.08	Digital I/O;	Digital I/O
16	P0.10/NFC2	Digital I/O;NFC2	Digital I/O;NFC2
17	P0.09/NFC1	Digital I/O;NFC1	Digital I/O;NFC1
18	P0.17	Digital I/O; SPI_CS	Digital I/O
19	P0.19	Digital I/O; SPI_CLK	Digital I/O
20	P0.20	Digital I/O; SPI_D0	Digital I/O
21	P0.21	Digital I/O; SPI_D1	Digital I/O
22	RESET	System Reset (Active low)	Reset
23	P0.22	Digital I/O; SPI_D2	Digital I/O
24	P0.23	Digital I/O; SPI_D3	Digital I/O
25	SWDIO	Hardware debug and Flash program I/O	Digital input

26	SWDCLK	Hardware Debug and Flash Program I/O	Digital I/O

8 PCB Design Guide

Please reserve empty area for PCB Antenna when you are going to aboard, device`s the empty range design minimum size :16.5*6.6mm , please kindly check the “PCB footprint and Dimensions” for reference.

9 PCB Footprint and Dimensions

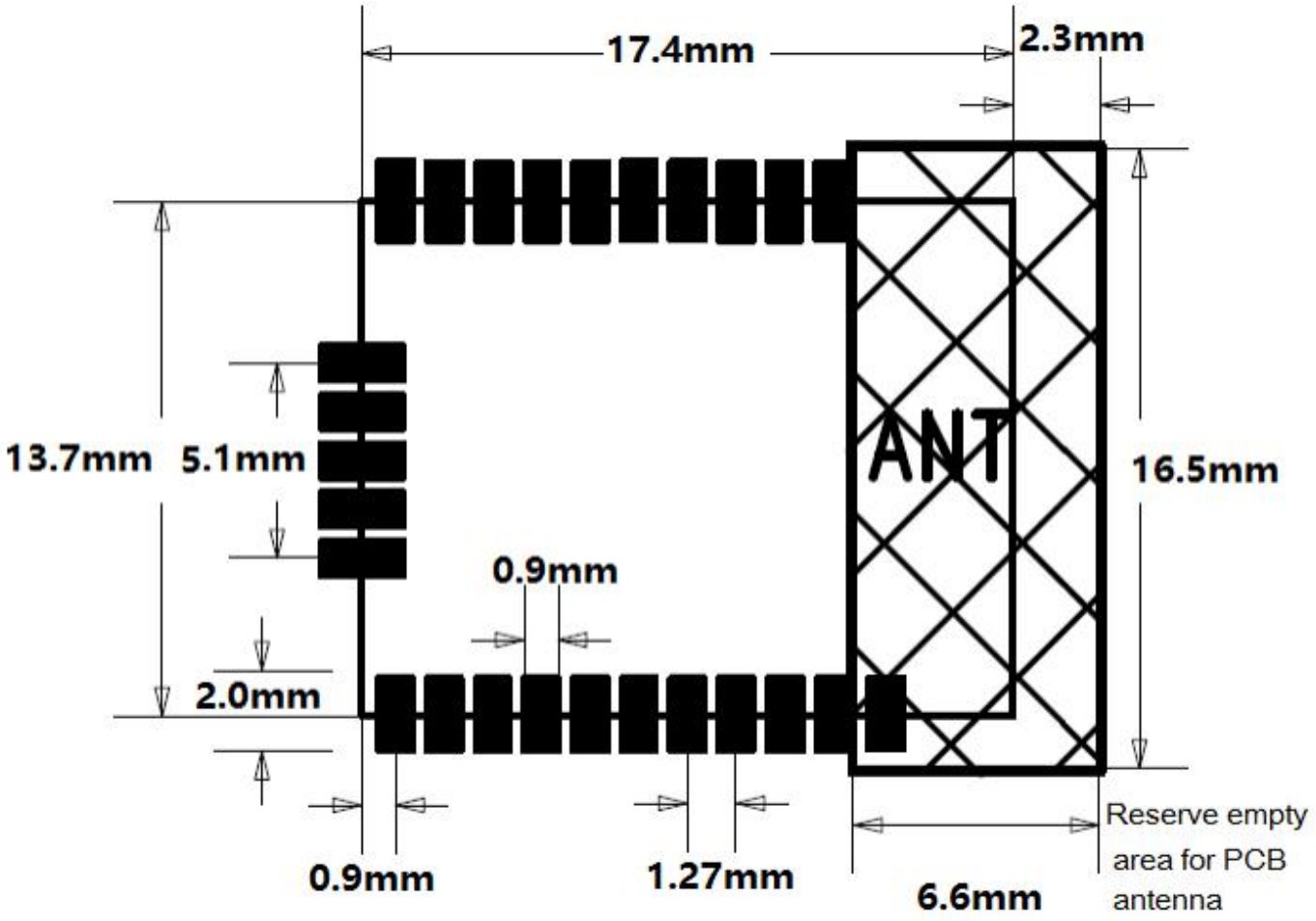

Figure 5: SSB501A Recommended PCB Footprint

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Storage Temperature Range		-40		125	°C
ESD Protection	VESD	/		4000	V
Supply Voltage	VCC	-0.3		3.9	V
Voltage On Any I/O Pin		-0.3		3.63	V

Table10-1: Absolute Maximum Ratings

*SSB501A series modules are Electrostatic Sensitive Devices and require special precautions while handling.

ESD precautions

The SSB501A series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the SSB501A series modules without proper ESD protection may destroy or damage them permanently.

The SSB501A series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, transportation and operation of any application that incorporates the SSB501A series module.

Don’t touch the module by hand or solder with non-anti-static soldering iron to avoid damage to the mod

10.2 Recommended Operation Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Extended Temp. Range	TA	-40	25	85	ºC
Power Supply	VCC	1.7	3.3	3.6	V
Input Low Voltage	VIL	0		0.3*VCC	V

Input High Voltage	VIH	0.7*VCC		VCC	V

Table10-2: Operating Conditions

10.3 Current

System State	TX Peak@4dBm	RX Peak	Sleep Mode（avg）	Idle Mode (avg)
Current (peak)@3V	7.5 mA	5.4 mA	0.4uA	1.2uA

Table10-3: Power Consumption in Different States

11 Manufacturing Process Recommendations

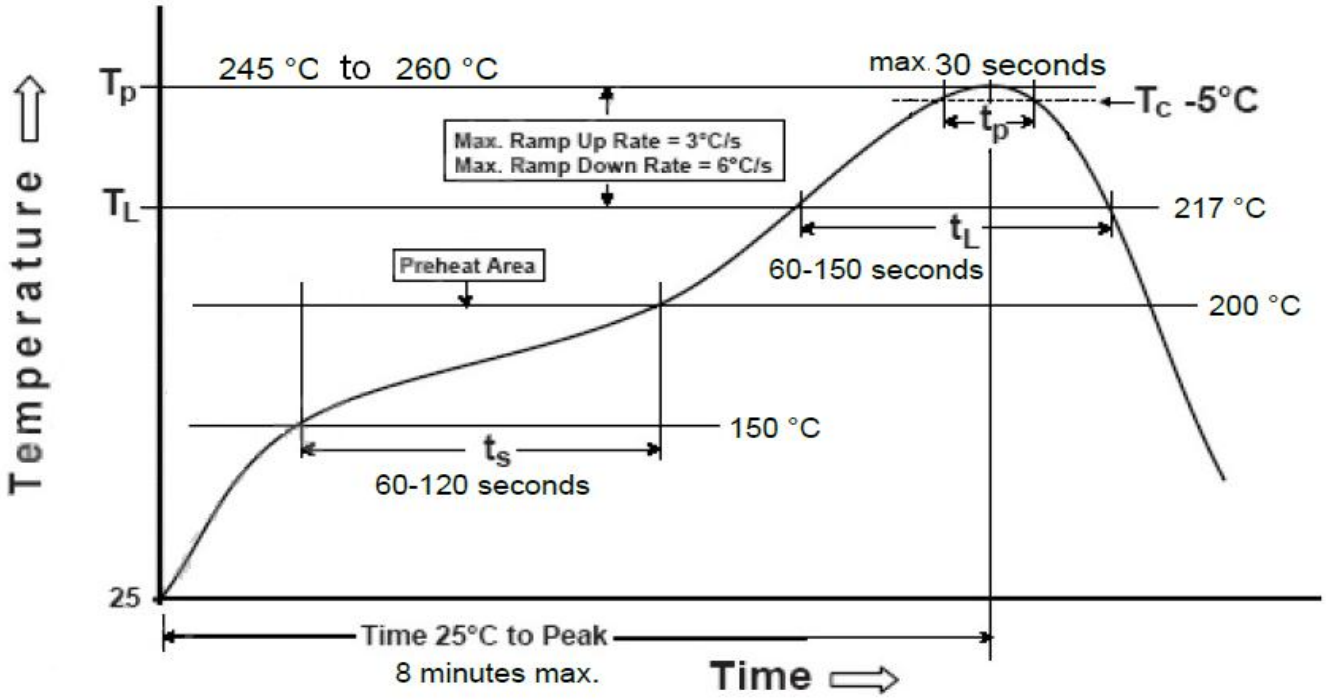

Figure 6: SSB501A Typical Lead-free Soldering Profile

Note： The final re-flow soldering temperature map chosen at the factory depends on additional external factors, for example, choice of soldering paste, size, thickness and properties of the module`s baseboard etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

12 Packaging Specification

SSB501A modules are put into tray and 528 units per tray. Each tray is ‘dry’ and vacuum packaging.

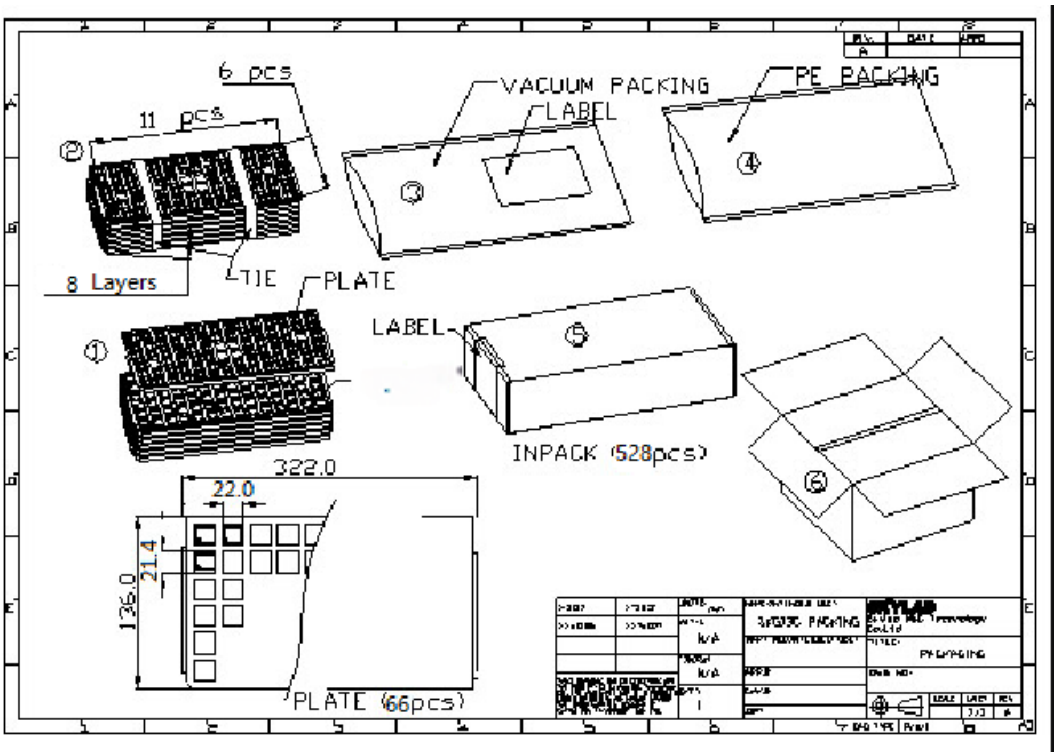

Figure 7: SSB501A Packaging

13 Ordering Information

Module No.	Crystal	Shielding	Antenna	Temperature Grade
SSB501A-CSPI	32.768K	Shielding	PCB	Industry
SSB501A-XXPI	No	No	PCB	Industry
SSB501A-CSEI	32.768K	Shielding	IPEX	Industry

14 Revision History

Revision	Description	Approved	Date
V1.01	Initial Release	George	20180525
V1.02	Update PCB Footprint and Dimensions	George	20180925
V1.03	Update Pin Description	George	20190201
V1.04	Update Pin16&Pin17 Description	George	20190321

V1.05	Update Pin12&Pin13 Description	Sherman	20191012