SSB1369A Multiprotocol Bluetooth 4.2/5.0 Low Energy Module Datasheet

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Revision History

Revision	Description	Approved	Date
V1.01	Initial Release	Benson	20180130
V1.02	Revise pin description name and description	Benson	20180718
V1.03	Revise PCB Footprint and Dimensions	Benson	20180907
V1.04	Add BLE 5.0 support	Kerry	20180911
V1.05	UpdateTransmit Power	Geoger	20200108

Contents

1. General Description

The SSB1369A is a highly integrated Bluetooth 4.2/5.0 BLE module, designed for high data rate, short-range wireless communication in the 2.4GHz ISM band. Also,SSB1369A support ANT Protocol. The module is based on Nordic nRF52810 radio Transceiver IC, has a 32 bit ARM Cortex-M4F CPU, Flash memory and analog and digital peripherals. The SSB1369A provides a low power and ultra-low cost BLE solution for wireless transmission applications.

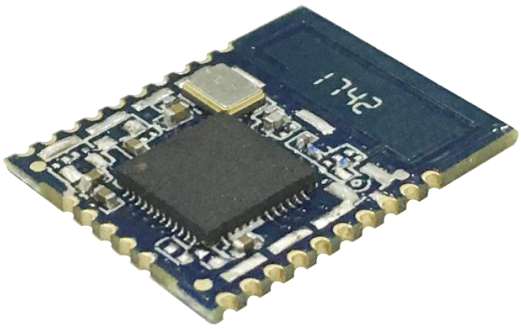

Figure 1: SSB1369A Top View

2. Applications

- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Interactive entertainment devices
  - Remote control
  - 3D Glasses
  - Gaming controller
- Personal Area Networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key-fobs + wrist watches
- Remote control toys
- Beacons
- Bluetooth Gateway
- Indoor Location
- Colourful LED Control

- Building automation
- Sensor networks.
- Asset tracking.

3. Features

- Main Chip: nRF52810
- Bluetooth® 4.2/5.0 low energy single-modeprotocol stack
  - L2CAP, ATT, GAP, GATT and SM protocols
  - Central and Peripheral roles
  - GATT Client and Server
  - Full SMP support including MITM and OOB pairing
- Support ANT Protocol
- Support BLE5.0. (Don’t support long range.)
- Supported data rates up to 1Mbps
- 8/10/12 bit ADC-6configurable channels
- 19 General Purpose I/O pins
- SPI Master/Slave
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- RoHS compliance (Lead-free)
- FCC,CE compliance

4. Application Block Diagram

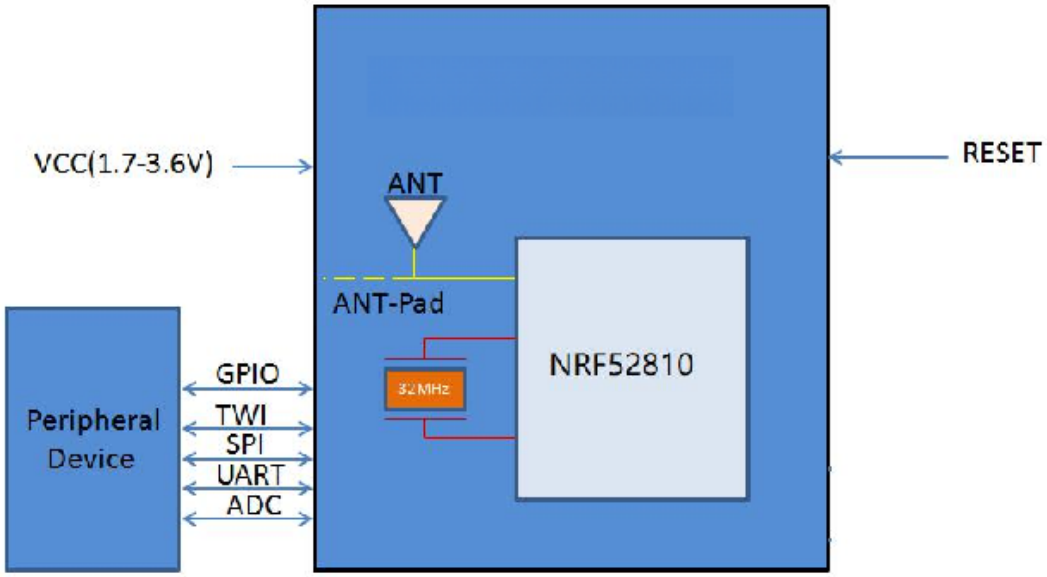

Figure 3: SSB1369A Block Diagram

5. Interfaces

Power Supply

Regulated power for the SSB1369A is required. The input voltage Vcc range should be 1.7V to 3.6V.

Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

System Function Interfaces

GPIOs

The general purpose I/O is organized as one port with up to 19 I/Os enabling access and control of up to 19 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

1、Input/output direction

2、Output drive strength

3、Internal pull-up and pull-down resistors

4、Wake-up from high or low level triggers on all pins

5、Trigger interrupt on all pins

6、All pins can be used by the PPI task/event system; the maximum number of pins that

can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

7、All pins can be individually configured to carry serial interface or quadrature demodulator signals

8、All pins can be configured as PWM signal.

9、There are 6 ADC/LPCOMP input in the 19 I/Os.

Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps ,250kbps and 400 kbps. The module has 2 TWI ports and they properties like following table.

Instance	Master/Slave
TWI0	Master
TWI1	Master

Table5-1: TWI Pin Share Scheme

Note： I2C:Inter－Integrated Circuit

Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple

slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line can be chosen from any GPIOs on the device and configed independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral support SPI mode 0,1,2,and 3.The module have 3 SPI ports and theirs they properties are as below:

Instance	Master/Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

Table5-2: SPI Properties

UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported.

Support the following baudrate in bps unit:
1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configed independently.

Analog to Digital Converter (ADC)

The 12 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

SKB369-AAXXPI Pin Number	Pin Number	Description
6	P0.28	Digital I/O; Analog input 4
7	P0.29	Digital I/O; Analog input 5
8	P0.30	Digital I/O; Analog input 6
9	P0.31	Digital I/O; Analog input 7
11	P0.02	Digital I/O; Analog input 2
12	P0.03	Digital I/O; Analog input 3

Table5-3: ADC Pins

Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Reset

The reset pin of the SSB1369A module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the parameters of the current setting will not be ANT .

6. Module Specifications

Hardware Features	
Model	SSB1369A
Antenna Type	PCB Antenna
Chipset Solution	nRF52810
Voltage	1.7V~3.6V
Dimension(L×W×H)	17.4×13.7×1.9 mm
Wireless Features	
Wireless Standards	Bluetooth ® 4.2/5.0,ANT
Frequency Range	2400MHz---2483.5MHz
Data Rates	1Mbps(Bluetooth ® 4.2); 2Mbps(Bluetooth ® 5.0)
Wireless Security	AES HW Encryption
Transmit Power	Tx Power -40dBm, -20dBm, -16dBm, -12dBm, -8dBm, -4dBm, 0dBm, +3dBm and +4dBm.
Work Mode	Central/Peripheral
Others	
Certification	RoHS
Environment	Operating Temperature: -40℃~85℃
	Storage Temperature: -40℃~125℃
	Operating Humidity: 10%~90% Non-condensing
	Storage Humidity: 5%~90% Non-condensing

7. Module Pinout and Pin Description

Module Pinout

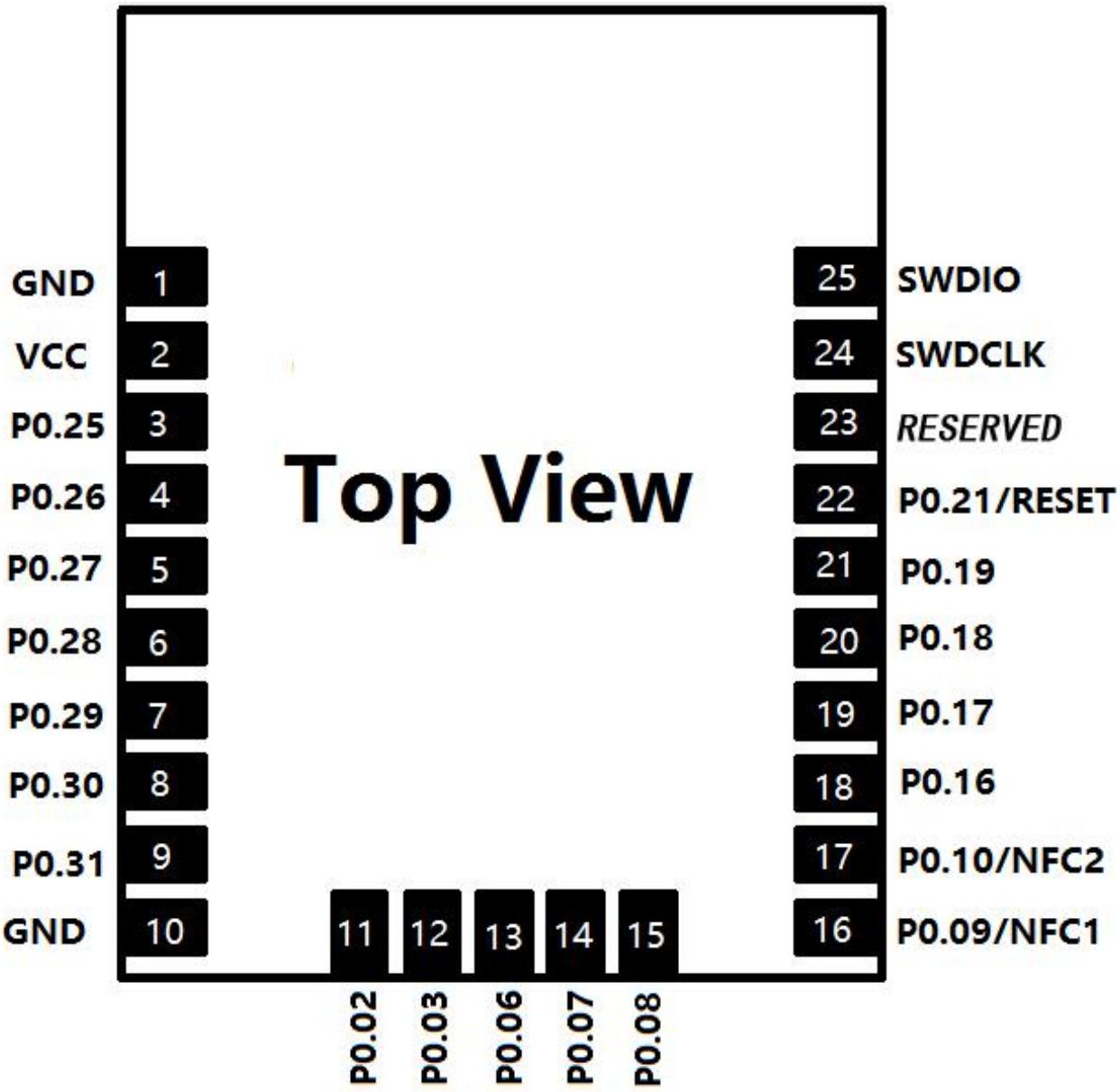

Figure 4: SSB1369A Module Pinout

Pin Description

Pin No.	Pin Name	Description	Remark
1	GND	Ground	
2	VCC	Main Power Supply	1.7V to 3.6V
3	P0.25	General Purpose I/O	Digital I/O
4	P0.26	General Purpose I/O	Digital I/O
5	P0.27	General Purpose I/O	Digital I/O
6	P0.28	Digital I/O; Analog input	ADC/LPCOMP input 4
7	P0.29	Digital I/O; Analog input	ADC/LPCOMP input 5
8	P0.30	Digital I/O; Analog input	ADC/LPCOMP input 6
9	P0.31	Digital I/O; Analog input	ADC/LPCOMP input 7
10	GND	Ground	
11	P0.02	Digital I/O; Analog input	ADC/LPCOMP input 0
12	P0.03	Digital I/O; Analog input	ADC/LPCOMP input 1
13	P0.06	General Purpose I/O	Digital I/O
14	P0.07	General Purpose I/O	Digital I/O
15	P0.08	General Purpose I/O	Digital I/O
16	P0.09	Digital I/O	Digital I/O;
17	P0.10	Digital I/O	Digital I/O;
18	P0.16	General Purpose I/O	Digital I/O
19	P0.17	General Purpose I/O	Digital I/O
20	P0.18	General Purpose I/O	Digital I/O
21	P0.19	General Purpose I/O	Digital I/O
22	P0.21/RESET	Digital I/O; System Reset (Active low)	Digital I/O; Reset
23	NC	Not Connect	
24	SWDCLK	Hardware debug and Flash program I/O	Digital input
25	SWDIO	Hardware Debug and Flash Program I/O	Digital I/O

8. PCB Design Guide

Please reserve empty area for PCB Antenna when you are going to design a device`s

board, the empty range minimum size :

16.5*6.6mm , please kindly check the “PCB footprint and Dimensions” for reference.

9. PCB Footprint and Dimensions

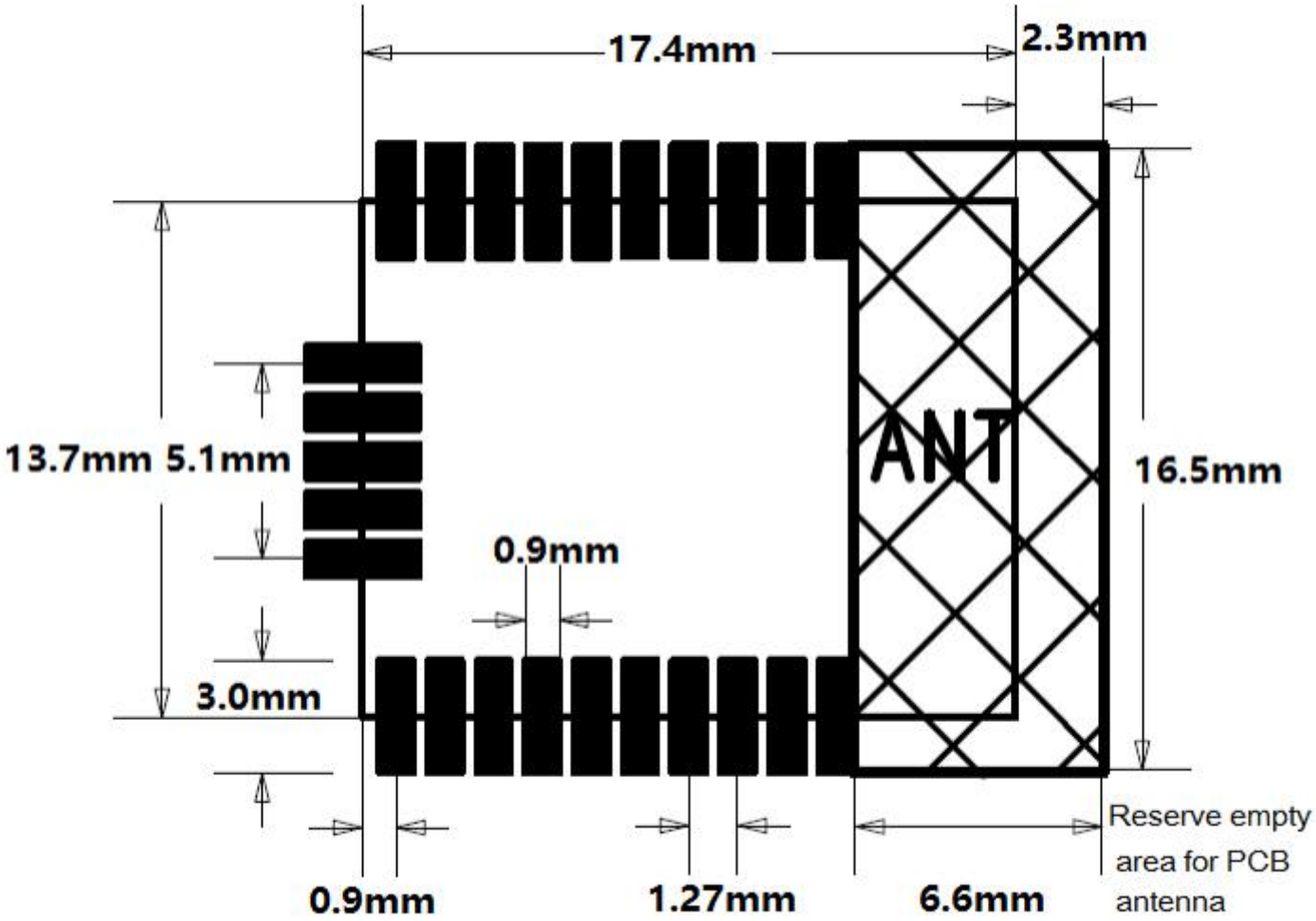

Figure 5:SSB1369A Recommended PCB Footprint

10. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Storage Temperature Range		-40		125	°C
ESD Protection	VESD	/		4000	V
Supply Voltage	VCC	-0.3		3.9	V
Voltage On Any I/O Pin		-0.3		3.63	V

Table10-1: Absolute Maximum Ratings

Recommended Operation Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Extended Temp. Range	TA	-40	25	85	ºC
Power Supply	VCC	1.7	3.3	3.6	V
Input Low Voltage	VIL	0		0.3*VCC	V
Input High Voltage	VIH	0.7*VCC		VCC	V

Table10-2: Operating Conditions

Current

System State	TX Peak @0dBm	RX Peak	Sleep Mode (avg)	Idle Mode (avg)
Current (peak)@3V	4.6 mA	4.6 mA	0.6uA	2.0uA

Table10-3: Power Consumption in Different States

11. Manufacturing Process Recommendations

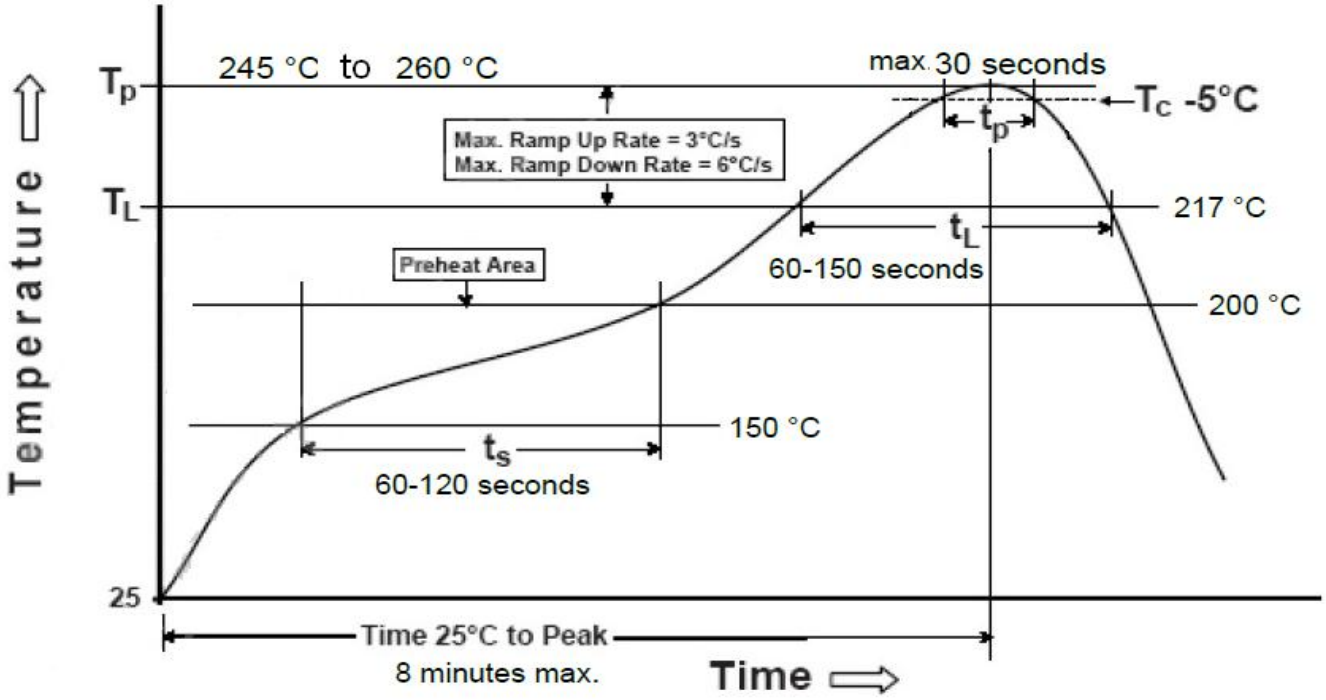

Figure 6: SSB1369A Typical Lead-free Soldering Profile

Note： The final re-flow soldering temperature map chosen at the factory depends on additional external factors, for example, choice of soldering paste,size, thickness and properties of the module`s baseboard etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

12. Packaging Specification

SSB1369A modules are put into tray and 528 units per tray. Each tray is ‘dry’ and vacuum packaging.

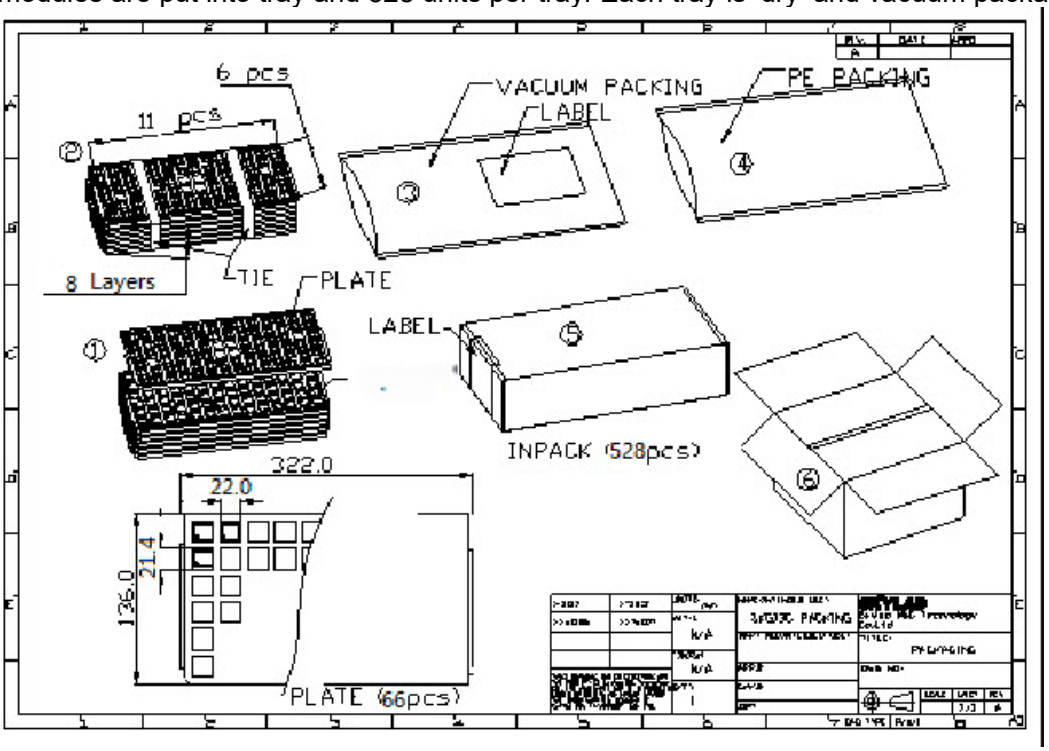

Figure 7: SSB1369A Packaging

13. Ordering Information

Module No.	Main chip	Crystal	Shielding	Antenna	Temperature Grade
SSB1369A	nRF52810	No	No	PCB	Industry